REMARKS

I. Introduction

Claims 1-6, 8 and 10-16 are pending. Claims 10, 12, 13 and 15 are allowed. Claims 1 and 16 remain rejected. Applicants note with appreciation the indication that claims 2 – 6, 8, 11, and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Rejections Under U.S.C. § 112

Claim 1 stands rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. In response to the Final Office Action, Applicants submitted, on February 1, 2008, three references which illustrate that having a scanner comprising only N-type MOS transistors was known and used in *conventional* NMOS (which do not include an AD converter) solid state imaging devices. In the Advisory Action, the Examiner did not consider Reference 1 (WO2004/025732A1) because the publication date was later than the filing date of the pending application. Regarding References 2 (JP 2003-163586) and 3 (JP 2003-249848), the Examiner asserts that Applicants did not clearly and distinctly point out where the references teach using N-type MOS transistors alone as transistors in a scanner.

Applicants submit herewith machine translations of References 2 and 3. A scanner (shift-register) comprising only N-type MOS transistors is described in paragraphs 01, 85, and 93, and is also depicted in Figure 2 of Reference 2. Additionally, such a scanner is described in paragraphs 01, 23, and 29 of Reference 3, and is also depicted in Figure 1.

In view of this evidence, withdrawal of this rejection is respectfully requested.

III. Claim Rejections Under 35 U.S.C. §§ 102 and 103

Claim 1 stands rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Gowda. Claim 16 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gowda in view of Kim. Applicants traverse these rejections for at least the following reasons.

Claim 1 is directed to a solid state imaging device using N-type MOS transistors alone as the transistors included therein. The solid state imaging device of claim 1 comprises, among other things, a comparison/storage unit provided correspondingly to each pixel column of a pixel unit for converting, into a digital signal, an analog signal output from an amplifying element included in each pixel belonging to a pixel row selected in the pixel unit, and for storing the digital signal. In NMOS solid state imaging devices, it is difficult to include an AD converter. As such, conventional NMOS solid state imaging devices do not perform to the level of CMOS solid state imaging devices which are able to incorporate an AD converter.

In rejecting claim 1, the Examiner relies on Gowda, which is expressly directed to a CMOS image sensor (see Abstract). Moreover, while the Examiner admits that the external circuitry associated with the imaging device taught by Gowda may comprise transistors other than N-type MOS transistors, the Examiner argues that "this is a moot point as the external circuitry in the form of the scanner taught in the current application has not been clearly illustrated as containing N-type MOS transistors alone." Thus, it appears that the Examiner's position is that while Gowda discloses non N-type MOS transistors, this is irrelevant (even though claim 1 explicitly recites using only N-type MOS transistors), because the scanner recited in claim 1 might contain non N-type MOS transistors.

There is no disclosure in the present application that the scanner described includes anything other than N-type MOS transistors. Moreover, as described above in reference to the rejection under 35 U.S.C. § 112, it was known in the art at the time of the invention to include a scanner having only N-type MOS transistors in a scanner of a NMOS solid state imaging device. In view of this general knowledge in the art and claim 1's specific recitation of a solid state imaging device using N-type MOS transistors alone, Applicants respectfully submit that Gowda, which discloses a CMOS solid state imaging device and which the Examiner acknowledges may comprise transistors other than N-type MOS transistors cannot anticipate claim 1. Applicants invention is directed to the problems associated with including an AD converter in an NMOS solid state imaging device, problems not existing with CMOS solid state imaging devices such as those described by Gowda.

Kim is also directed to a CMOS solid state imaging device. As such, Kim fails to overcome the deficiencies of Gowda. Accordingly, claim 16, which depends from claim 1, is patentable over the cited references for at least the reasons described references at least for the same reasons described above in reference to claim 1.

IV. Conclusion

In view of the above remarks, Applicants submit that this application should be allowed and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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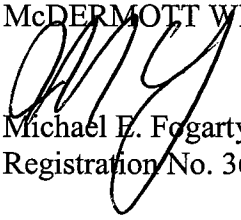

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